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APPLICATION FOR U.S. LETTERS PATENT

Title:
PROCESS FOR MANUFACTURING INTEGRATED CHEMICAL MICROREACTORS OF SEMICONDUCTOR MATERIAL

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PROCESS FOR MANUFACTURING INTEGRATED CHEMICAL MICROREACTORS OF SEMICONDUCTOR MATERIAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application Serial Number 09/874,382, filed June 4, 2001, entitled "Process for Manufacturing Integrated Chemical Microreactors of Semiconductor Material," and claims priority to EP 00830400.8, filed June 5, 2000, and each is incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] Not applicable.

REFERENCE TO A COMPACT DISK APPENDIX

[0003] Not applicable.

BACKGROUND OF THE INVENTION

[0004] As is known, the treatment of some fluids involves an increasingly precise temperature regulation, in particular when chemical or biochemical reactions are involved. Furthermore, it is frequently necessary to use very small amounts of fluid, since the fluid is costly or not always readily available.

[0005] This is, for example, the case of the DNA-amplification process (polymerase chain reaction process, also called a PCR process) wherein precise temperature control in the various phases (it is necessary to repeatedly perform preset thermal cycles), the need to avoid as far as possible thermal gradients in the reaction areas of the fluid (to have uniform temperature in these areas), and also the quantity of fluid used (which is very costly) are of crucial importance for obtaining good reaction efficiency or even for obtaining the reaction itself.

[0006] Other examples of treatment of fluids having the characteristics indicated above are, for instance, linked chemical and/or pharmacological analyses, biological tests, etc.

[0007] At present, various techniques are available that enable thermal control of chemical or biochemical reagents. A first technique uses a reactor including a glass or plastic base on which a biological fluid is deposited through a pipette. The base rests on a hot-plate called "thermo-chuck," which is controlled by external instrumentation.

[0008] Another known reactor comprises a heater, which is controlled by appropriate instrumentation and on which a biological fluid to be examined is deposited. The heater is supported by a base which also carries a sensor arranged in the immediate vicinity of the heater and is also connected to the instrumentation for temperature regulation, so as to enable precise control of the temperature.

[0009] Both types of reactors are often enclosed in a protective casing.

[0010] A common disadvantage of the known reactors lies in the large thermal mass of the system; consequently, they are slow and have high power absorption. For example, in the case of the PCR process mentioned above, times of the order of 6-8 hours are required.

[0011] Another disadvantage of known solutions is linked to the fact that, given the macroscopic dimensions of the reactors, they are able to treat only relatively high volumes of fluids (i.e., minimum volumes of the order of milliliters).

[0012] The disadvantages referred to above result in very high treatment costs (in the case of the aforementioned PCR process, the cost can amount to several hundreds of dollars); in addition, they restrict the range of application of known reactors to test laboratories alone.

[0013] To overcome the above mentioned drawbacks, starting from the late eighties miniaturized devices of reduced thermal mass have been developed and allow a reduction in the times required for completing the DNA-amplification process.

[0014] The first of these devices is described in the article by M.A. Northrup, M.T. Ching, R.M. White, and R.T. Watson, "DNA amplification with a microfabricated reaction chamber," Proc. 1993 IEEE Int. Conf. Solid-State Sens. Actuators, pp. 924-926, 1993, and comprises a reactor cavity formed in a substrate of monocrystalline silicon by anisotropic etching. The bottom of the cavity comprises a thin silicon-nitride membrane, on the outer edge of which are heaters of polycrystalline silicon. The top part of the cavity is sealed with a glass layer. Thanks to its small thermal mass, this structure can be heated at a rate of 15°C/sec., with cycling times of 1 minute. With this device it is possible to carry out, for a volume of fluid of 50 μl,

twenty amplification cycles in periods approximately one fourth the time required by conventional thermocyclers and with a considerably lower power consumption.

[0015] However, the described process (as others currently used based on bonding of two silicon substrates previously subjected to anisotropic etches in KOH, TMAH, or other chemical solutions) is costly, has high critical aspects and low productivity, and is not altogether compatible with the usual manufacture steps used in microelectronics.

[0016] Other more recent solutions includes forming, inside a first wafer of semiconductor material, buried channels connected to the surface via inlet and outlet trenches, and, inside a second wafer of semiconductor material, reservoirs formed by anisotropic etching, and bonding together of the two wafers.

[0017] Also this solution, however, is disadvantageous in that the process is costly, critical, has low productivity, and requires the use of a glass frit for bonding the two wafers together.

BRIEF SUMMARY OF THE INVENTION

[0018] The aim of the present invention is therefore to provide a process allowing integration of reservoirs in a single integrated device that includes the chemical microreactor. According to one embodiment of the invention, an integrated microreactor is provided, having a semiconductor material body, one or more buried channels extending in the semiconductor material body at a distance from the surface, first and second trenches extending from the surface respectively as far as first and second ends of the buried channels, and a resist layer extending above the surface and defining first and second reservoirs connected to the first and second trenches. A process for the fabrication of an integrated microreactor is encompassed by the invention, including forming a semiconductor material body having one or more buried channels, forming first and second trenches extending from the surface of the semiconductor body as far as, respectively, first and second ends of the buried channels and forming first and second reservoirs above the surface, respectively connected to the first and second trenches. A method for the use of a microreactor is also described as part of the invention. The method includes introducing a fluid from a reservoir into a reactor cavity, where the reactor cavity is a buried channel extending in a semiconductor material body at a distance from a surface of the semiconductor material body, where the reservoir is formed in a resist layer on the surface of the semiconductor material body, and where the fluid is introduced via a trench extending from the

reservoir on the surface of the semiconductor material body as far as one end of the buried channel, then heating the fluid within the reaction chamber, and cooling the fluid within the reaction chamber. This method may also include removal of the fluid from the reaction chamber into a second reservoir, also formed in the resist layer on the surface of the semiconductor material body where the fluid may be sampled by the use of a sensing electrode for the presence of a product of the method.

BRIEF SUMMARY OF THE DRAWINGS

[0019] For a better understanding of the present invention, two preferred embodiments thereof are now described, simply as non-limiting examples, with reference to the attached drawings, wherein:

[0020] Figures 1-5 show cross-sections through a wafer of semiconductor material in successive manufacturing steps of a microreactor according to a first embodiment of the invention;

[0021] Figure 6 shows a top view of the wafer of Figure 5;

[0022] Figures 7 and 8 show cross-sections similar to those of Figures 1-5, in final manufacturing steps; and

[0023] Figures 9-12 show cross-sections through a wafer of semiconductor material in successive manufacturing steps of a microreactor according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Figure 1 shows a wafer 1 comprising a semiconductor body 2, typically of monocrystalline silicon, accommodating buried channels 3 extending parallel to a surface 4 of the semiconductor body 2. Preferably, as indicated in the top view of Figure 6 by dashed lines, a plurality of buried channels 3 extend parallel to one another at short distances. In this case, the buried channels 3 may have an approximately circular or rectangular section and are arranged at a distance of 50 μm from one another and at a depth of 20-30 μm from the surface 4. When the buried channels 3 have a rectangular cross-section, they have an area of 30 μm x 200 μm, and a length of 10 mm, and the total area occupied by the buried channels 3 is 50 mm^2. Alternatively, it is possible to have a single channel, approximately 10 mm in length, approximately 5 mm in

width, and approximately 20 μm in height. In both cases, a total volume is obtained of approximately 1 mm^3 (1 μl).

[0025] A first insulating layer 5, for example of silicon dioxide, extends on top of the surface 4 of the semiconductor body 2 and accommodates a polycrystalline-silicon heating element 10. Preferably, the heating element 10 extends substantially over the area occupied by the buried channels 3, but not over the longitudinal ends of the buried channels 3, where inlet and outlet openings of the channels 3 are to be formed, as described hereinafter.

[0026] Contact regions 11, for example of aluminum, extend through openings of the first insulating layer 5 and are in electrical contact with two opposite ends of the heating element 10 to enable passage of electric current through the heating element 10 and heating of the underlying area.

[0027] A sensing electrode 12 formed by a multilayer, for example of aluminum, titanium, nickel and gold, in a per se known manner and thus not described in detail, extends on top of the first insulating layer 5, laterally shifted with respect to the buried channels 3.

[0028] A second insulating layer 13, for example of TEOS (tetra-ethyl orthosilicate) oxide extends on top of the first insulating layer 5 and has an opening through which the sensing electrode 12 protrudes.

[0029] The wafer 1 of Figure 1 is obtained, for example, as described below. Initially, the buried channels 3 are formed, preferably according to the teaching of European patent applications 99830206.1 of May 9, 1999, and 00830098.0 of February 11, 2000, filed by the present applicant and incorporated herein for reference. Initially, a substrate of monocrystalline silicon is time etched in TMAH to form the channels 3. Then the channels 3 are preferably coated with a material inhibiting epitaxial growth, and a monocrystalline epitaxial layer is grown on top of the substrate and of the channels. The epitaxial layer closes at the top the buried channels 3 and forms, together with the substrate, the semiconductor body 2 in which, if so envisaged, control electronic components may be integrated at the sides of the buried channels.

[0030] Subsequently, and in succession, the following steps are performed: the bottom portion of the first insulating layer 5 is deposited on the surface 4; a polycrystalline silicon layer is deposited and defined so as to form the heating element 10; the top portion of the

first insulating layer 5 is formed; openings are made in the first insulating layer 5; an aluminum layer is deposited and defined to form the contact regions 11 and the bottom region of the sensing electrode 12; the second insulating layer 13 is deposited and then removed from the area corresponding to the sensing electrode 12; and next the aluminum, titanium, nickel and gold regions forming the sensing electrode 12 are formed.

[0031] Subsequently (Figure 2), a protective layer 15 is formed. For this purpose, a layer of standard positive resist may be deposited, for example including three components, formed by a NOVOLAC resin, a photosensitive material or "pac" (photo-active compound), and a solvent, such as ethylmethyl ketone and lactic acid, used normally in microelectronics for the definition of integrated structures. Alternatively, another compatible material may be used, which can be defined and is capable of resisting etching both of the silicon of the semiconductor body 2 and of the material still to be deposited on top of the protective layer 15, such as a TEOS oxide, in which case the protective layer 15 blends with the second protective layer 13.

[0032] Next (Figure 3), the protective layer 15 is defined and, where the protective layer 15 has been removed, the second insulating layer 13 and first insulating layer 5 are etched. In this way, an inlet opening 16a and an outlet opening 16b are obtained that extend as far as the surface 4 of the semiconductor body 2 and are basically aligned to the longitudinal ends of the channels 3. The inlet opening 16a and outlet opening 16b preferably have a length of approximately 5 mm (in a direction perpendicular to the plane of the drawing) and a width of approximately 60 μm.

[0033] A resist layer 18 is then deposited (Figure 4), in the example illustrated the resist being negative and having a thermal conductivity of between 0.1 and 1.4 W/m°K and a thermal expansion coefficient TEC $\leq$ 50 ppm/°K, such as the material known under the name "SU8" (Shell Upon 8) produced by SOTEC MICROSYSTEMS. For example, the resist layer 18 has a thickness of between 300 μm and 1 mm, preferably 500 μm.

[0034] Subsequently (Figure 5), the resist layer 18 is defined so as to form an inlet reservoir 19 and an outlet reservoir 20. In particular, and as shown in the top view of Figure 6, wherein the channels 3 are represented by dashed lines, the outlet reservoir 20 is formed as an extension of the outlet opening 16b (and thus is connected to the ends of the channels 3 close to the sensing electrode 12) and encompasses the sensing electrode 12. The inlet reservoir 19 is formed, instead, as an extension of the inlet opening 16a, and is thus connected to the opposite

ends of the channels 3. Preferably, the reservoirs 19, 20 have a length (in a direction perpendicular to the plane of Figure 5) of approximately 6 mm; the inlet reservoir 19 has a width (in a horizontal direction in Figure 5) of between 300 μm and 1.5 mm, preferably approximately 1 mm, so as to have a volume of at least 1 mm3, and the outlet reservoir 20 has a width of between 1 and 4 mm, preferably of approximately 2.5 mm.

[0035] Next (Figure 7), using as masking layer the resist layer 18 and the protective layer 15, access trenches 21a and 21b are formed in the semiconductor body 2 by performing a trench etching. In particular, the access trenches 21a and 21b extend aligned to the inlet and outlet openings 16a, 16b, from the surface 4 as far as the channels 3, so as to connect the channels 3 to one another in parallel, as well as to the inlet reservoir 19 and the outlet reservoir 20.

[0036] Finally, the exposed portion of the protective layer 15 is removed, so as to expose the sensing electrode 12 again (Figure 8), and the wafer 1 is cut into dice to obtain a plurality of microreactors.

[0037] According to a different embodiment, the inlet and outlet reservoirs are formed in a photosensitive dry-resist layer. In this case, the access trenches can be made before applying the photosensitive, dry resist layer.

[0038] According to an implementation of this embodiment, wherein parts corresponding to those of the first embodiment are designated by the same reference numbers, the process starts from a wafer 1, as shown in Figure 2, comprising the semiconductor body 2, in which the buried channels 3 have already been formed. The first insulating layer 5, the heating element 10, the contact regions 11, the sensing electrode 12, the second insulating layer 13, and the protective layer 15 are also already formed on the semiconductor body 2.

[0039] Subsequently (Figure 9), using a special masking layer (not shown), the protective layer 15, the second insulating layer 13, the first insulating layer 5, and the semiconductor body 2 are etched to form inlet openings 27a and outlet openings 27b at the ends of the buried channels 3. In practice, the inlet opening 27a of Figure 9 corresponds to the opening 16a and the trench 21 a of Figure 7, and the outlet opening 27b of Figure 9 corresponds to the opening 16b and the trench 21b of Figure 7. If so required, the wafer 1 may be planarized.

[0040] Subsequently (Figure 10), a resist layer 28 is applied. Here the resist layer 28 is made of a photosensitive dry resist, of the type currently used for printed circuits, wherein the photosensitive dry resist, supplied in rolls of various sizes and thicknesses, is applied to the base coated with a copper layer, and is then laminated and thermocompressed. According to the invention, preferably a photosensitive dry resist layer is used of an opposite type with respect to the protective layer 15 (here negative) having a thickness of between 500 μm and 1 mm, which is made to adhere to the wafer 1 by lamination at a temperature of 105-118°C and is cut according to the external profile of the wafer 1.

[0041] The resist layer 28 is then exposed (using a special mask), developed and etched so as to form the inlet reservoir 19 and the outlet reservoir 20, thus obtaining the structure shown in Figure 11. Finally, the uncovered portion of the protective layer 15 is removed so as to expose the sensing electrode 12 again (Figure 12).

[0042] The advantages of the described process and device are the following. First, an integrated microreactor formed in a single piece may be obtained, without bonding two wafers of silicon and/or glass together. The process involves steps that are usual in microelectronics, with decidedly lower costs than the current ones. The process is moreover far from critical, affords high productivity, and does not require the use of materials (such as "glass flit") which are difficult to use on account of their deformability.

[0043] The method of operation of the device is as follows according to one embodiment of the invention. The buried channels 3 function as a reactor cavity. A reactive fluid is introduced into the inlet reservoir 19 and thence into the buried channels 3 via the access trench 21a. This may be accomplished by capillary action or by appropriate air pressure, or other acceptable techniques. In the case of a PCR operation, the fluid is heated and cooled repeatedly according to specific parameters, which parameters may be custom for each particular applications and fluid type. The setting of such parameters is within the skill of those in the art. The heating is accomplished by the use of the heating element 10 as described herein. The cooling step may be carried out by removing the heat and permitting the fluid to cool towards the ambient. Cooling may be accelerated by the use of a heat sink attached in a known manner to the semiconductor body 2. Other cooling means may be employed as appropriate, for example, a cooling fan or by the circulation of a liquid coolant.

[0044] At the conclusion of the heating and cooling cycles the fluid is removed from the buried channels 3 via the access trench 21b, into the outlet reservoir 20, by the application of air pressure, or by other means as appropriate. In some cases the fluid may be removed from the outlet reservoir 20 for further processing. In one embodiment, the sensing electrode 12 is employed to detect a desired product of the reaction process in the fluid. This detection process is within the skill of those practiced in the art, and so will not be described in detail.

[0045] Having the sensor electrode 12 in the same semiconductor substrate and adjacent to the channel 3 is advantageous for certain types of such processes. Of course, other process sequences do not employ such a sensor 12 and it does not need to be used in all embodiments of the invention.

[0046] Finally, it is clear that numerous variations and modifications may be made to the process and to the microreactor described and illustrated herein, all falling within the gist of the invention, as defined in the attached claims. For example, the type of resist used for forming the resist layer and the protective layer may be different from the ones described herein. For instance, the protective layer 15 may be made with a negative, instead of positive, resist or with another protective material resistant to the etching of the resist layer and of the silicon, and selectively removable with respect to the second insulating layer 13; and the resist layer may be made with a positive resist, instead of a negative one. Instead of a plurality of buried channels, it is possible to make a single buried channel of appropriate dimensions, for example applying the technique described in the aforementioned European Patent Application 99830206.1 and timeetching the silicon of the semiconductor body 2 extending between the buried channels 3 so as to form a single cavity having a width equal to that of the trenches 21 a, 21b or of the openings 27a, 27b. In addition, in the second embodiment, the resist layer 28 may be replaced by two layers, the bottom layer having a function of support for the top one.

[0047] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

[0048] What is claimed is: